CLAIMS

What is claimed is:

1. A processing system comprising:

an application processor having a first graphics interface;

a coprocessor having a second graphics interface to communicate pixel-stream formatted graphics command data and pixel-stream formatted image data with the application processor, the coprocessor also having a display interface to provide display data to a graphics display; and

a high-speed datapath between the first graphics interface and the second graphics interface.

2. The processing system of claim 1 wherein the first graphics interface comprises first drivers to receive graphics command data from a processing core of the application processor and to format the graphics command data into the pixel-stream formatted graphics command data,

wherein the second graphics interface comprises second drivers to reformat the pixel-stream formatted graphics command data back to the graphics command data,

wherein the first drivers and the second drivers comprise at least one of either hardware or software components, and

wherein the high-speed datapath comprises a pair of conductors to carry high-speed digital differential signals.

3. The processing system of claim 1 wherein the coprocessor further comprises a coprocessor processing core responsive to the graphics command data and image data to generate the display data for the graphics display.

4. The processing system of claim 1 wherein the coprocessor comprises a graphics accelerator to offload at least some graphics-processing operations from the application processor, the graphics-processing operations including at least one of two-dimensional (2D) graphics operations, three-dimensional (3D)

graphics operations, multimedia encoding and decoding operations, and display refresh operations, the at least some graphics-processing operations indicated by the graphics command data.

5. The processing system of claim 1 wherein the graphics command data comprises commands to instruct the coprocessor to perform graphics-processing operations including at least one of two-dimensional (2D) graphics operations, three-dimensional (3D) graphics operations, multimedia encoding and decoding operations, and display refresh operations.

6. The processing system of claim 1 further comprising a system bus and a system memory, wherein the application processor has a memory controller to access the system memory over the system bus, and wherein the coprocessor has a system memory interface to access the system memory over the system bus.

7. The processing system of claim 6 wherein the application processor further comprises on-die memory therein, the application processor performs a DMA transfer of graphics data from the on-die memory to the coprocessor over the high-speed datapath, and the application processor refrains from transferring the graphics data to the coprocessor over the system bus.

8. The processing system of claim 1 wherein the coprocessor is an integrated part of the graphics display.

9. The processing system of claim 8 wherein the graphics display comprises photodiodes to generate image data of a scanned image, and the coprocessor converts the image data to pixel-stream formatted image data for transfer over the high-speed datapath to the application processor.

10. The processing system of claim 1 wherein the display data describes pixels of the graphics display in a per-pixel format, and wherein the pixel-stream formatted image data comprises pixel data in a pixel format, and wherein the pixel-stream formatted command data comprises command data in a pixel format.

11. The processing system of claim 1 wherein the coprocessor comprises one of a graphics accelerator, a hardware accelerator, or a companion device.

12. The processing system of claim 1 further comprising:

an omnidirectional antenna to receive communication signals; and

a receiver to translate the communication signals to data signals for the application processor, the communication signals including graphics data,

the application processor generates the graphics command data from the received graphics data, and transfers the pixel-stream formatted graphics command data over the high-speed datapath to the coprocessor, the coprocessor reformats the pixel-stream formatted graphics command data and generates display data for display by the graphics display.

13. The processing system of claim 12 comprising one of either a personal digital assistant (PDA) or a wireless telephone.

14. The processing system of claim 1 comprising a general processing system.

15. A communication device comprising:

an application processor having a first interface;

a coprocessor having a second interface to receive formatted command data and formatted output data from the application processor, the coprocessor also having an output interface to provide output data to an I/O device; and

a high-speed datapath to communicate the formatted command data and formatted output data between the first interface and the second interface.

16. The device of claim 15 wherein the first interface comprises first drivers to receive command data from a processing core of the application processor and to format the command data into the formatted command data,

wherein the second interface comprises second drivers to reformat the formatted command data back to the command data,

wherein the first drivers and the second drivers comprise hardware and software components, and

wherein the high-speed datapath comprises a pair of conductors to carry high-speed digital differential signals.

17. The device of claim 15 wherein the coprocessor further comprises a coprocessor processing core responsive to the command data and output data to generate the output data for the I/O device.

18. The device of claim 15 further comprising a system bus and a system memory, and wherein the application processor has a memory controller to access the system memory over the system bus, and wherein the coprocessor has a system memory interface to access the system memory over the system bus.

19. The device of claim 18 wherein the application processor further comprises on-die memory, the application processor performs a DMA transfer of data from the on-die memory to the coprocessor over the high-speed datapath, and the application processor refrains from transferring the data to the coprocessor over the system bus.

20. The device of claim 15 wherein the I/O device includes RF circuitry to interface with an antenna for communication of RF signals, the application processor and coprocessor communicate at least one or either digitally encoded data or digitally encoded voice signals over the high-speed datapath, wherein wireless transceiver functions are allocated between the applications processor and the coprocessor for wireless communications.

21. A method comprising:

formatting graphics command data into a pixel-stream format;

sending the pixel-stream formatted graphics command data along with pixel-stream formatted image data from a first graphics interface of an application processor over a high-speed datapath to a second graphics interface of a coprocessor;

reformatting the pixel-stream formatted graphics command data at the coprocessor back to graphics command data; and

generating, by the coprocessor, display data for a graphics display from the graphics command data and image data received over the high-speed datapath.

22. The method of claim 21 further comprising, prior to sending, buffering the pixel-stream formatted graphics command data, and wherein sending comprises programming a DMA descriptor to send the pixel-stream formatted graphics command data from the buffer along with pixel-stream formatted image data to the coprocessor.

23. The method of claim 21 further comprising refraining, by the application processor, from sending the graphics command data along with pixel-stream formatted image data to the coprocessor over a system bus.

24. The method of claim 21 wherein generating display data comprises performing graphics-processing operations including at least one of two-dimensional (2D) graphics operations, three-dimensional (3D) graphics operations, multimedia encoding and decoding operations, and display refresh operations.

25. A communication system comprising:

an omnidirectional antenna to receive communication signals;

a receiver to translate the communication signals to data signals; and

a processing system having an application processor and a coprocessor coupled by a high-speed datapath,

wherein the application processor receives the data signals and generates and sends data-stream formatted graphics command data and data-stream formatted image data to the coprocessor over the high-speed datapath, the coprocessor having a display interface to generate and to provide display data for a graphics display.

26. The system of claim 25 wherein the first graphics interface comprises first drivers to receive graphics command data from a processing core of the application processor and to format the graphics command data into the data-stream formatted graphics command data,

wherein the second graphics interface comprises second drivers to reformat the data-stream formatted graphics command data back to the graphics command data,

wherein the first drivers and the second drivers comprise at least one of either hardware or software components, and

wherein the high-speed datapath comprises a pair of conductors to carry high-speed digital differential signals.

27. The system of claim 25 wherein the coprocessor further comprises a coprocessor processing core responsive to the graphics command data and image data to generate the display data for the graphics display.

28. The system of claim 25 wherein the coprocessor comprises a graphics accelerator to offload at least some graphics-processing operations from the application processor, the graphics-processing operations including at least one of two-dimensional (2D) graphics operations, three-dimensional (3D) graphics operations, multimedia encoding and decoding operations, and display refresh operations, the at least some graphics-processing operations indicated by the graphics command data.